Self-Aligned Indium–Gallium–Zinc Oxide Thin-Film Transistor With Source/Drain Regions Doped by Implanted Arsenic

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***Abstract*—Self-aligned top-gate amorphous indium–gallium–zinc oxide (a-IGZO) thin-film transistors (TFTs) with source/drain (S/D) regions doped by implanted arsenic are developed in this letter. The resulting a-IGZO TFTs exhibit much better thermal stability than those with S/D regions doped by hydrogen or argon plasma. They also show good electrical performance, including field-effect mobility of 12 $\mathrm{cm^2/V \cdot s}$, threshold voltage of 3.5 V, subthreshold swing of 0.5 V/dec, and ON/OFF current ratio of 9×10^7.**

***Index Terms*—Amorphous indium–gallium–zinc oxide (a-IGZO), arsenic, self-aligned, thin-film transistors (TFTs).**

I. INTRODUCTION

RECENTLY, thin-film transistors (TFTs) based on zinc oxide [1] and its variants, such as amorphous indium–gallium–zinc oxide (a-IGZO) [2]–[5], have been pursued as replacements of the silicon-based TFTs for flat-panel display applications due to their higher mobility and larger area uniformity, as compared with amorphous silicon (a-Si) and polycrystalline silicon (p-Si) TFTs. The conventional a-Si TFTs, which are used as switching devices in active-matrix liquid crystal displays, have the advantages of low manufacturing cost and large area uniformity. However, their low field-effect mobility ($< 1\ \mathrm{cm^2/V \cdot s}$) may be not sufficient to drive active-matrix organic light-emitting diode (AMOLED). Due to their high mobility ($> 50\ \mathrm{cm^2/V \cdot s}$) and electrical stability, the conventional p-Si TFTs are currently used as driving devices in AMOLED displays. However, the main issues are the nonuniformity of their field-effect mobility and threshold voltage, which are caused by the grain size and grain boundaries in p-Si thin films.

In order to realize system-on-panel technology for large-size, high-resolution, and low-cost AMOLED flat-panel displays, the development of self-aligned top-gate oxide TFTs with good electrical performance and high stability is necessary. The conventional bottom-gate structure is unsuitable for the system-on-panel application due to the high parasitic capacitance and poor scalability. Several oxide TFTs with self-aligned top-gate structure were reported, in which source/drain (S/D) regions were doped by hydrogen diffusion from silicon nitride by plasma-enhanced chemical vapor deposition (PECVD) [6], hydrogen plasma treatment [7]–[9], or argon plasma treatment [10]. However, hydrogen can rapidly diffuse in the a-IGZO thin films at a temperature above 150 °C. A large amount of hydrogen diffuses out of the S/D regions or into the channel region, which lead to poor performance. The oxygen vacancies in the S/D regions caused by argon plasma treatment will decrease after thermal annealing, which increase the sheet resistance of the S/D regions. Thus, thermal stability is a main issue for a-IGZO TFTs with S/D regions formed by argon or hydrogen plasma treatments [6].

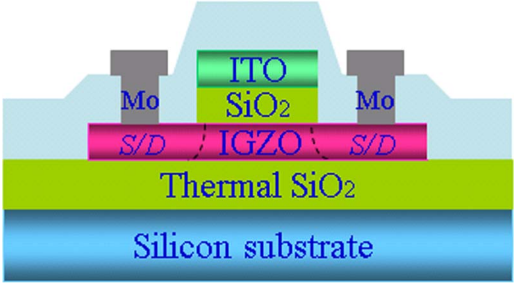

Fig. 1. Cross-section schematic of the proposed self-aligned top-gate a-IGZO TFT.

In this letter, self-aligned top-gate a-IGZO TFTs with S/D regions doped by implanted arsenic has been fabricated and characterized. The proposed a-IGZO TFTs show good electrical performance and high thermal stability.

II. EXPERIMENTAL

The cross-sectional schematic of the self-aligned top-gate type a-IGZO TFT studied in this letter is shown in Fig. 1.

A 100-nm-thick IGZO active layer was first sputtered on thermally oxidized silicon wafer by dc magnetron sputtering using a target of $In_2O_3 : Ga_2O_3 : ZnO = 1{:}1{:}1$ mol% in a mixed argon and oxygen ambient at room temperature. The deposition pressure and the power were 2 mtorr and 120 W, respectively. The IGZO thin film was amorphous from the X-ray diffraction (XRD) pattern. After patterning this a-IGZO active layer by a liftoff process with an acetone solution, a 120-nm-thick SiO_2 layer as a gate dielectric was deposited by

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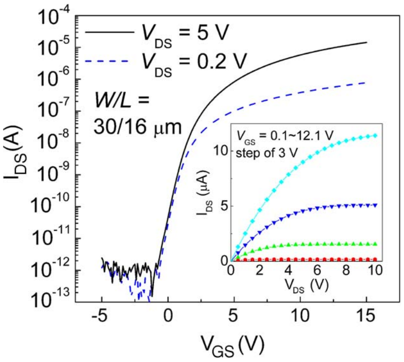

Fig. 2. Transfer and output characteristics (shown in the inset) of the proposed self-aligned top-gate a-IGZO TFTs.

PECVD on top of the a-IGZO layer at 300 °C. A 230-nm-thick indium tin oxide (ITO), which was used as a gate electrode, was sequentially sputtered at room temperature and then defined using photolithography and liftoff process. Then, an annealing process was executed at 200 °C for 30 min in N_2 and O_2 ambient. The S/D regions were self-aligned implanted with arsenic at a dose of $5 \times 10^{15}/\text{cm}^2$ and energy of 100 keV using a gate-electrode ITO pattern as a mask. An annealing process at 525 °C for 30 min in O_2 ambient was performed to activate the implanted arsenic dopant. After this annealing process, the IGZO thin film was still amorphous from the XRD pattern. The gate dielectric above the S/D regions was dry etched using CF_4/O_2 plasma. After that, an Al_2O_3 thin film was deposited as a passivation layer by the dc magnetron sputtering technique at room temperature. After forming the contact holes, a 200-nm-thick Mo layer was deposited by sputtering and patterned as gate/S/D electrodes. The electrical properties of the a-IGZO TFTs were measured using an HP4156A precision semiconductor parameter analyzer in air.

III. RESULTS AND DISCUSSION

Fig. 2 shows the typical transfer and output characteristics of the fabricated a-IGZO TFTs with a width-to-length ratio of 30 μm/16 μm. They exhibit good transfer TFT characteristics at a drain-to-source voltage V_{DS} of 0.2 V, such as field-effect mobility of 12 $\text{cm}^2/\text{V} \cdot \text{s}$, threshold voltage of 3.5 V, subthreshold swing of 0.5 V/dec, and ON/OFF current ratio of 9×10^7. The gate leakage current for the proposed a-IGZO TFTs was less than 10 pA. The output characteristic shows clear linear regions and does not show significant current crowding at low V_{DS}, indicating that low series resistance R_{SD} in S/D contacts were obtained. In the a-IGZO thin film with implanted arsenic, arsenic substitution on the zinc site could introduce a donor state, assuming a formal oxidation state of $+3$ for arsenic on the Zn^{+2} site [11]. The oxygen ambient during the activation process (at 525 °C for 30 min) was to avoid the generation of oxygen vacancies in the a-IGZO thin film. On the contrary, the a-IGZO thin films without arsenic implantation show large resistance after the CF_4/O_2 plasma treatment. Thus, this low S/D series resistance in the proposed a-IGZO TFTs is caused by the implantation and activation of the arsenic dopant.

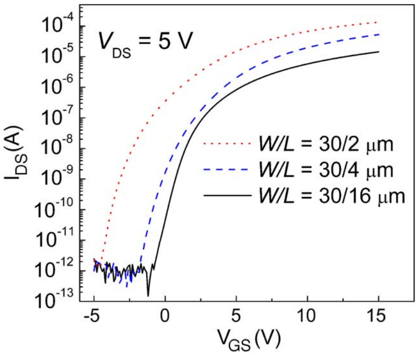

Fig. 3. Transfer characteristics of the a-IGZO TFTs with the same channel width but different channel lengths.

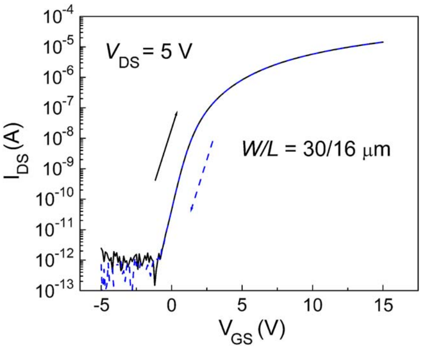

Fig. 4. Hysteresis characteristic of the a-IGZO TFTs.

To study the scaling-down behaviors of the proposed a-IGZO TFTs, the transfer characteristic (at $V_{DS} = 5$ V) of the proposed a-IGZO TFTs with different channel lengths ($L = 16$, 4, and 2 μm) are compared in Fig. 3. From Fig. 3, for the devices with channel lengths of 16 and 4 μm, a small change of the threshold voltage and little degradation of subthreshold swing were obtained, which indicates that the a-IGZO TFTs scales down nicely with channel lengths for $L \geq 4$ μm. For the device with a channel length of 2 μm, the threshold voltage shifted largely. This may be due to the lateral diffusion of the arsenic dopant into the channel region, which caused short-channel effects. As the channel length decreased from 16 to 2 μm, the maximum field-effect mobility of the a-IGZO TFTs decreased from 12 to 8.5 $\text{cm}^2/\text{V} \cdot \text{s}$. The decrease of the field-effect mobility for short-channel devices is due to the existence of the S/D series resistance on the potential distribution across the channel.

To investigate the effect of the SiO_2 gate dielectric and its interface with an active layer, the hysteresis of a-IGZO TFTs was examined, as shown in Fig. 4. Little shift of the threshold voltage for the hysteresis loop indicated that little electrons were trapped at or near the SiO_2/a-IGZO interface or within the a-IGZO channel layer.

Fig. 5(a) shows the evolution of transfer characteristics for the proposed a-IGZO TFTs with S/D regions doped by implanted arsenic before and after heat treatment at 200 °C for 20 min. No degradation of electrical performance was observed. However, the performance of a-IGZO TFTs with S/D regions doped by argon or hydrogen plasma can easily degrade after heat treatment at 200 °C, as shown in Fig. 5(b). The hydrogen

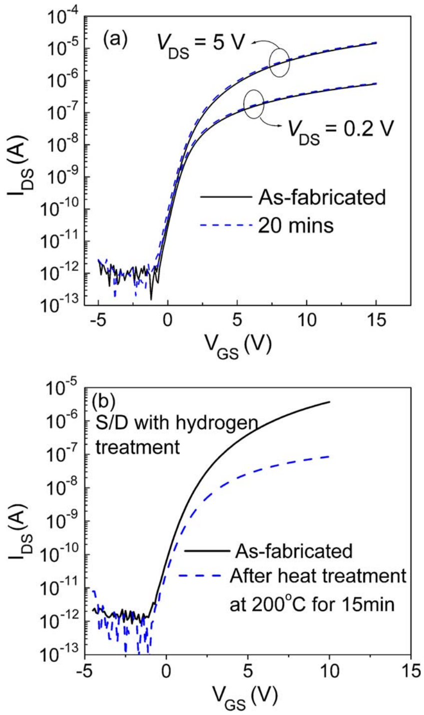

Fig. 5. Evolution of transfer characteristics of the a-IGZO TFTs with S/D regions doped with (a) arsenic and (b) hydrogen under heat treatment at 200 °C.

in the S/D regions diffuses rapidly out of the S/D regions with a large diffusion coefficient [12], which leads to large series resistance in S/D regions of the device. Thus, the ON-current I_{DS} dramatically decreased. The mobility decreased from 10 to 0.09 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, the ON/OFF current ratio decreased from 4×10^6 to 8×10^5, and the subthreshold swing increased from 0.6 to 0.7 V/dec. It demonstrates that the proposed a-IGZO TFTs with arsenic-doped S/D regions have much better thermal stability than those with argon or hydrogen plasma treatment.

IV. CONCLUSION

Self-aligned top-gate a-IGZO TFTs with arsenic-doped S/D regions have been developed in this letter. The resulting transistor exhibits field-effect mobility of 12 $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$, threshold voltage of 3.2 V, subthreshold swing of 0.5 V/dec, and ON/OFF current ratio of 9×10^7. The proposed a-IGZO TFTs also show much better thermal stability, as compared with those with S/D regions formed by hydrogen or argon plasma treatments.

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